Find our project on GitHub! https://github.com/ThePomelo/Spectrum-Sensing

SDR - Spectrum Sensing

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Project Overview

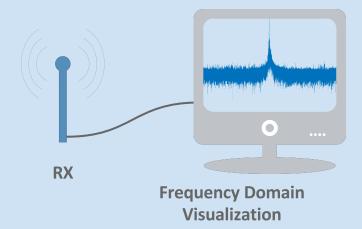
Project Goal

TX

Develop a platform for visualizing the radio frequency spectrum using software-defined radio.



Time Domain Radio Signals



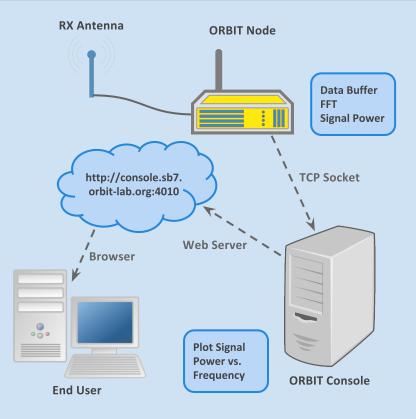
Project Objectives

- Using ORBIT, configure radio receiver(s) to collect IQ time samples
- Process the samples to obtain frequency-domain data
- Analyze frequency data to identify any unknown signals
- Repeat with modified receiver carrier frequency, sampling rate, etc. to scan the available frequency spectrum for signals
- Implement methods above in real-time on CPU and FPGA

Current Progress

CPU Implementation

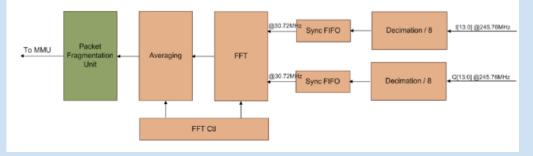
- Browser-based visualization using Wt C++ library
- Configured Sandbox 7 and Grid consoles
- Plan to use TCP sockets to send FFT data from receiver node to console
- Console will display data in web browser



Current Progress

FPGA Implementation

- Spectrum Sensing Application (Sensing across a large bandwidth)
- Design of PFU (Packet Fragmentation Unit)
- Implementation of state machines in VHDL
- The final project goal is to use Octave in Linux to detect the spectrum



```
WHEN ST DATA =>
o busy \leq '0';
IF(sig valid = '1') THEN
  IF(UNSIGNED(wrd cnt) = 0) THEN
    o sof \langle = '1' \rangle;
  END IF;
  IF(i eof = '1') THEN
    sig busy <= '1';
    sig last pkt <= '1';</pre>
    current state <= ST LAST WORD;</pre>
  ELSE
     IF(UNSIGNED(wrd cnt) = X"FE") THEN
       sig busy \langle = '1' \rangle;
       current state <= ST LAST WORD;
     END IF;
  END IF;
  o data <= i data;
  o data en <= i data en;
  wrd cnt <= STD LOGIC VECTOR(UNSIGNED(wrd cnt)+ 1);</pre>
END IF:
```

Achievements

- Design of ORBIT Grid Experiments using OEDL scripts
- Development of MATLAB Spectrogram Toolkit for postprocessing signals
- Development of Real-Time Plotting Module in C++ for the Wiserd Framework
- Browser-based Visualization for plotting module
- Design of a Mealy finite-state machine of the PFU using VHDL code

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